REMARKS/ARGUMENTS

The present Amendment is in response to the Office Action having a mailing date of March 23, 2005. Claims 1-27 are pending in the present Application. Applicant has amended claims 1, 4, 10, and 13. Applicant has also added claims 28-30. Consequently, claims 1-30 remain pending in the present Application.

Applicant has amended claims 1 and 10 to recite that the transistors are configured such that they have the same state during a read operation. Support for the amendment can be found in paragraph 26, lines 8-12. Applicant has amended claims 4 and 13 to replace "read line" with second electrically conductive line and third electrically conductive line, respectively. New claims recite that the transistors are connected to an uninterrupted electrically conductive path to ground during reading. Support for the amendment can be found in Fig. 6, items 160, 165, 150, and 180. Accordingly, Applicant respectfully submits that no new matter is added.

In the above-identified Office Action, the Examiner objected to claim 4 because the term "read line" lacked proper antecedent basis. Applicant notes that claim 13 had a similar defect. Applicant has amended claims 4 and 13 to recite second electrically conductive line and third electrically conductive line, respectively. Consequently, the terms in claims 4 and 13 have proper antecedent basis. Accordingly, Applicant respectfully submits that the Examiner's objection to claim 4 has been addressed.

In the above-identified Office Action, the Examiner rejected claims 1-6, 8-16, and 18-26 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,717,844 (Ohtani). In so doing, the Examiner cited Figure 1, items 7 and 9 as teaching the transistors coupled in parallel. With respect to claim 20, which recites that all of the plurality of transistors are "on" during reading, the

Examiner cited Ohtani, col. 4, lines 62-64 as teaching that the plurality of transistors (7 and 9 in Ohtani) are on.

Applicant respectfully traverses the Examiner's rejection. Claim 1 recites a device including spin-dependent tunneling cells, as well as first, second, and third electrically conductive lines. The first and second electrically conductive lines are disposed adjacent to one of the cells. The third electrically conductive line is electrically connected to the cell to read the states of the cell, as well as being connected to a plurality of transistors in parallel. Claim 1 further recites that transistors are configured to have a same state during a read operation. Claim 10 recites an analogous device including a spin-dependent tunneling cell, a first electrically conductive line adjacent to a ferromagnetic element of the cell, and a second electrically conductive line. Claim 10 further recites that the second electrically conductive line is connected to a plurality of transistors in parallel and the plurality of transistors being configured to have a same state during a read operation. Similarly, claim 20 recites the use of an electrically conductive read line that is connected to a plurality of transistors in parallel, and is used to read a cell when the transistors are all turned on.

Thus, claims 1, 10, and 20 each recite an electrically conductive line that is used in reading and that is coupled to transistors that are in parallel and that have the same state during read operations. Claim 20 recites that this state is the "on" state.

In contrast, Ohtani fails to teach or suggest a device in which the line used in reading is coupled to transistors that are in parallel and that all have the same state during a read operation. The transistors of *Ohtani* are not configured to have the same state during a read operation. Ohtani expressly states that during reading, the WE signal is low. Ohtani, col. 5, lines 54-58. Consequently, the transistor 9 would be turned off. Ohtani also states that the transistor 6 is on and

that the transistor 7 can be turned on for some states of the cells. Ohtani, col. 5, lines 57-60 and col. 5, line 65-col. 6, line 3. Consequently, during a read operation, the transistors cited by the Examiner as corresponding to the recited plurality of transistors may have differing states. This is true despite the Examiner's citation of col. 4, lines 63-64 of Ohtani, which merely indicate that nodes N1 and N2 of Ohtani can be used to read the states of the cells of Ohtani. Consequently, Ohtani fails to teach or suggest the devices recited in independent claims 1, 10, and 20. Accordingly, Applicant respectfully submits that claims 1, 10, and 20 are allowable over the cited references.

Claims 2-6 and 8-9 depend upon independent claim 1. Claims 11-16 and 18-19 depend upon independent claim 10. Claims 21-26 depend upon independent claim 20. Consequently, the arguments herein apply with full force to claims 2-6, 8-9, 11-16, 18-19, and 21-26. Accordingly, Applicant respectfully submits that claims 2-6, 8-9, 11-16, 18-19, and 21-26 are allowable over the cited references.

In the above-identified Office Action, the Examiner also rejected claims 7, 17, and 27 under 35 U.S.C. § 103 as being unpatentable over Ohtani in view of U.S. Patent No. 6,775,183 (Heide). Claims 7, 17, and 27 depend upon independent claims 1, 10, and 27, respectively. For at least the reasons stated above, *Ohtani* fails to teach, disclose, or suggest each and every element of Claims . In particular, Ohtani fails to teach or suggest the use of transistors which are connected to a line used in reading in parallel, and which are configured to have the same state during a read operation.

Heide fails to remedy the defects of Ohtani. Applicant can find no mention in Heide of connecting a reading line to transistors that are coupled in parallel. Moreover, Heide is devoid of mention of the transistors having the same state during a read operation. Consequently, any combination of Ohtani and Heide would fail to include this feature. Stated differently, if the

teachings of Heide were added to those of Ohtani, the device 13 of Ohtani might include the materials mentioned in the cited portion of Heide: multilayers of GeMn/NiFe/GeMn, NiFe/GeMn/NiFe, Fe/FeSi/Fe, and Fe(Ni)Zr/CrO_2/Fe(Ni)Zr. However, the combination would still not include transistors that are connected in parallel and have the same state during a read operation. In addition, although Heide describes the use of metallic ferromagnetic materials, and ferromagnetic semiconductor materials, Heide does not describe the use of half-metallic ferromagnets such as PtMnSb, NiMnSb, Co_2MnSi, or Sr_2FeMoO_6. For the above reasons, Ohtani in view of Heide fails to teach or suggest the devices recited in claims 7, 17, and 27. Accordingly, Applicant respectfully submits that claims 7, 17, and 27 are allowable over the cited references.

New claims 28-30 are allowable as currently presented. Claims 28-30 recite that the transistors are configured to be connected to an uninterrupted path to ground during reading. Ohtani and Ohtani in view of Heide fail to teach or suggest such devices. Ohtani describes transistors 7 and 9 in Figure 1 of Ohtani that are connected in parallel. However, these transistors do not provide an uninterrupted path to ground during reading. Instead, the transistors 11 and 12 provide a path to ground for particular cells 13 and 14, respectively. Consequently, Ohtani fails to teach or suggest connected a plurality of transistors to an uninterrupted path to ground. Similarly, Applicant can find no mention in Heide of connecting transistors in parallel and to an uninterrupted path to ground during reading. Consequently, any combination of Ohtani and Heide fails to teach or suggest this feature. Accordingly, Applicant respectfully submits that claims 28-30 are allowable as currently presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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August 23, 2005
Date

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